Amendments to the Drawings:

The attached sheets of drawings designate the figures as –Prior Art--. These sheets, which includes Figs. 1A, 1B, 1C, 2A, 2B, and 3, replaces the original sheet including Figs. 1A, 1B, 1C, 2A, 2B, and 3.

Attachment: Replacement Sheets

REMARKS

Claims 10-14 and 17-24 are currently pending. Claims 1-9, 15-16, and 25 are cancelled. Claim 18 is amended. Reconsideration of presently pending claims 10-14 and 17-24 is respectfully requested in light of the above amendments and the following remarks.

Objection to Specification

The examiner objects to paragraph 21 of the current specification due to minor errors. Amendments have been made to the specification to correct the errors. Accordingly, Applicants respectfully request the withdrawal of the objection to the specification.

Objection to Drawings

The examiner objects to Figs. 1A-1C, 2A-2B, and 3 of the current specification. Replacement sheets have been submitted to designate the figures as –Prior Art--. Accordingly, Applicants respectfully request the withdrawal of the objection to the Figs. 1A-1C, 2A-2B, and 3.

Rejections under 35 U.S.C. §102(b), Claims 10-14, 17-24

Claims 10-14, and 17-24 are rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Okazawa (US Patent Publication No. 2002/0034117A1 hereinafter referred to as "Okazawa") as supported by Tran (U.S. Patent No. 6356,477B1).

The PTO provides in MPEP § 2131 that

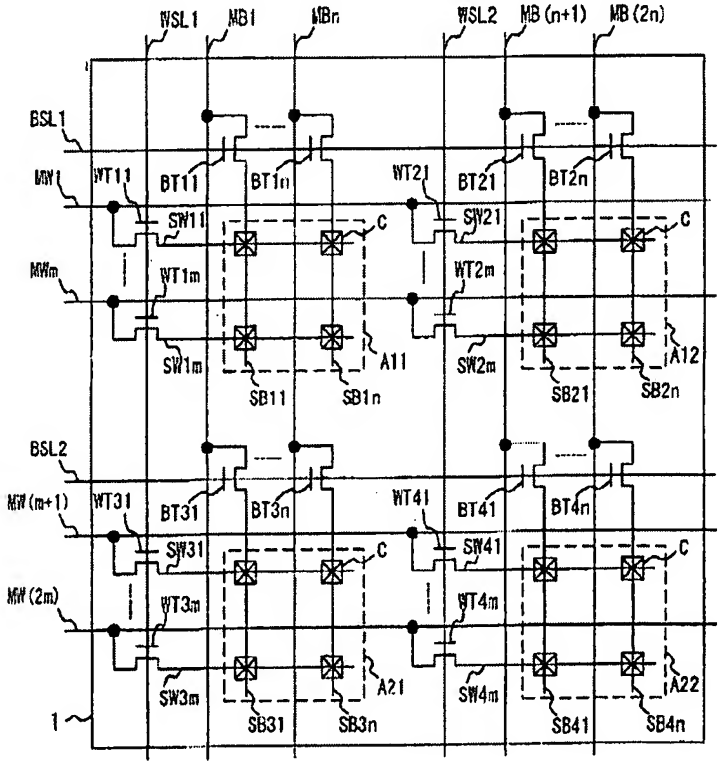
> *"[t]o anticipate a claim, the reference must teach every element of the claim...."*

Therefore, with respect to claim 10, to sustain this rejection the Okazawa patent must contain all of the above claimed elements of the claim. However, contrary to the examiner's position that all elements are disclosed in the Okazawa reference, the reference does not disclose "first diodes, each first diode comprising a cathode, and an anode coupled to a corresponding bit line; second diodes, each second diode comprising an anode, and a cathode coupled to a

corresponding word line; and magnetic tunnel junction memories including a pinned layer; a free layer; and a non-magnetic layer located between the pinned layer and the free layer; each magnetic tunnel junction memory being positioned at a crossing point of a bit line and a word line, each magnetic tunnel junction memory being connected between a first diode at a corresponding crossing bit line and a second diode at a corresponding crossing word line."

Fig. 4 of Okazawa is shown below:

FIG. 4



As shown in Fig. 4, Okazawa discloses word selecting transistors, such as WT11, WT12, and bit selecting transistors, such as BT 11, BT12. Okazawa does not disclose first diodes, each first diode comprising a cathode, and an anode coupled to a corresponding bit line or second diodes, each second diode comprising an anode, and a cathode coupled to a corresponding word line, let alone a magnetic tunnel junction memory that is connected between a first diode at a

corresponding crossing bit line and a second diode at a corresponding crossing word line. In fact, none of the figures in Okazawa shows the use of diodes or a connection of the magnetic tunnel junction memory with a diode. Therefore, Okazawa does not disclose the features of claim 10.

The examiner alleges in the office action that it is inherent that the source to drain of such transistor will effectively function as a diode (i.e. intrinsic diode). The examiner further alleges that Tran supports the fact that transistors having intrinsic diodes can be replaced by diodes for the purposes of blocking sneak/reverse currents in memory array (Figs. 4 and 10). Applicants respectfully disagree. According to MPEP section 2163.07(a), which states:

> "To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed.Cir. 1999) (Emphasis added).

Thus, it must be clear that the use of diodes is necessarily present in the thing described in Okazawa. However, Okazawa fails to disclose that the use of diodes is necessarily present in the arrangement as shown in Fig. 4 above. To the contrary, Okazawa specifically discloses the use of transistors in the thing. The mere possibilities or probabilities of using diodes may not be used to establish inherency. Therefore, it is not inherent that the source to drain of such transistor will effectively function as a diode, as alleged by the examiner.

In addition, the Tran reference is irrelevant in a rejection under 35 U.S.C. §102(b). But for the sake of argument, the diodes as disclosed by Tran for blocking sneak/reverse currents in the memory array are not "first diodes, each first diode comprising a cathode, and an anode coupled to a corresponding bit line, and second diodes, each second diode comprising an anode, and a cathode coupled to a corresponding word line," as recited in claim 10. Figs. 4 and 5 of Tran are shown below:

FIG. 4

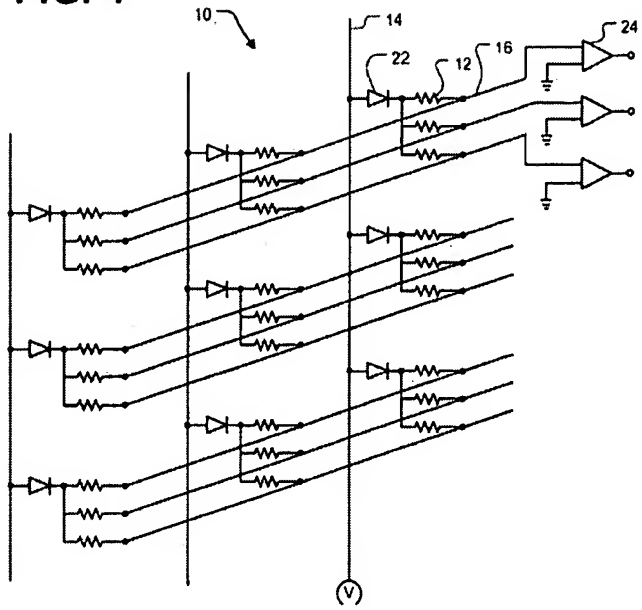
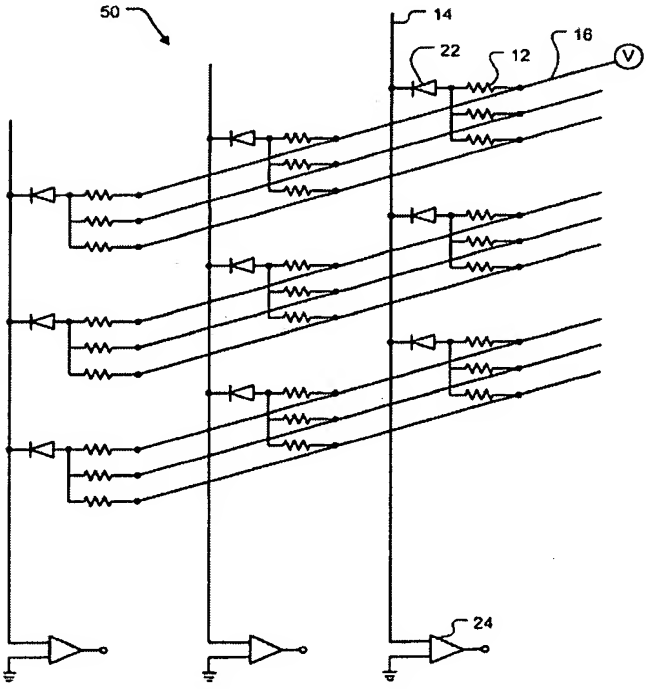


FIG. 5



In Fig. 4, Tran discloses diodes that comprise an anode coupled to a selected word line 14, and a cathode coupled to memory element 12, which connects to amplifiers 24. In Fig. 5, Tran discloses diodes that comprise a cathode coupled to a selected word line 14, which connects to amplifiers 24, and an anode that is coupled to memory element 12. Thus, Tran only discloses diodes comprising either an anode or a cathode that is either coupled to a selected word line or a memory element. None of Tran's diodes comprises an anode that is coupled to a corresponding bit line, as recited in claim 10. Therefore, not only that it is not inherent the source to drain of such transistor will effectively function as a diode, the diodes for blocking sneak/reverse currents in the memory array as disclosed by Tran still do not comprise an anode coupled to a corresponding bit line, as recited in claim 10. Claim 17 and amended claim 18 recite similar features also not disclosed by Okazawa or Tran. Accordingly, Applicants respectfully request the withdrawal of the rejection to claims 10-14 and 17-24 under 35 U.S.C. §102(b).

Conclusion

It is clear from all of the foregoing that independent claims 10, 17, and 18 are in condition for allowance. Dependent claims 11-14 and 19-24 depend from and further limit independent claims 1, and therefore are allowable as well.

An early formal notice of allowance of claims 10-14 and 17-24 is requested.

Respectfully submitted,

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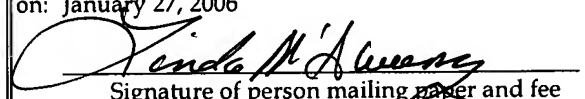

Signature of person mailing paper and fee